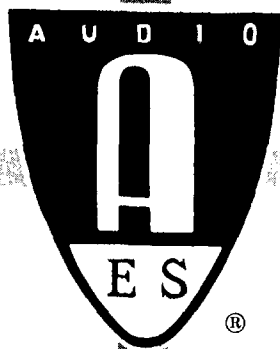


A TRANSISTORIZED PROFESSIONAL TAPE RECORDER

by  
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## A TRANSISTORIZED PROFESSIONAL TAPE RECORDER

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### INTRODUCTION

The transistorized electronics for the model AG-350 tape recorder system is described in this paper. The solid state version succeeds the vacuum tube electronics supplied with the previous system. A major requirement of the new design was to preserve the quality, operating features and flexibility of the vacuum tube predecessor, and to improve upon it wherever possible.

Generally, the design task was the usual one of shaping response, and obtaining the required power at the reproduce output and record head while maintaining a wide dynamic range commensurate with professional tape recorders.

This problem is more acute using transistors rather than vacuum tubes, because the relatively low power supply voltage usually limits the level of signal voltage that can be handled without clipping. The clip-to-signal ratio (overload margin) may be improved to any desired degree by selecting a lower signal voltage as the normal operating level. However, a lower operating level results in the signal being closer to equipment noise, and the signal-to-noise ratio is impaired.

If the noise of the circuitry can be held to a sufficiently low level, an operating level can be chosen so that both the clip-to-signal and signal-to-noise ratios meet the design goals. Previous experience with transistorized tape recorders of various kinds had shown that, from the standpoint of being able to operate in a stable manner with low noise, silicon planar transistors were ideal for the amplification of low level audio signals. However, it was not until these transistors were manufactured by automatic methods and encapsulated in plastic, rather than being housed in hermetically sealed cases, that their cost became comparable with vacuum tubes. This important development made it practical to manufacture high quality transistorized tape recorders for other than military or specialized uses.

This paper discusses the problems of designing a recorder capable of recording at any of six tape speeds from 3-3/4 ips to 30 ips, with domestic or international versions of equalization, and with the widely varying record characteristics of the types of tapes in use today. Each equalizer is capable of being contained in a small plug-in housing. Two such housings for two different tape speeds with a relay to select the desired equalization are provided.

The units treated will be: (1) in the reproduce section--the reproduce preamplifier, reproduce calibration amplifier and line amplifier; and (2) in the record section--the record calibration amplifier, record equalization circuit, record head amplifier, and the erase and bias oscillator. The design of the regulated power supply will be described, as well as the methods used to prevent audible disturbances being recorded on the tape when the record section is turned on or off.

### REPRODUCE AMPLIFIER SECTION

#### The reproduce preamplifier (Figure 1)

Gain and signal-to-noise ratio required much attention in the design at the reproduce preamplifier, because the signal obtainable from the reproduce head is very low (2.5 mv from 1/2 track head at 700 cps). The signal at the output of the preamplifier should be at least 110 mv for all frequencies (after equalization is applied), so that in the following stage it will not be difficult to maintain the signal-to-noise ratio achieved to this point. A higher preamplifier output would be too close to the power supply ceiling, and would result in a reduced overload margin.

In this design, there is sufficient open loop gain (over 75 db) in the first three stages to provide the desired output level--after generous feedback (accomplished at the same time as equalization) at low audio frequencies. This ensures that an adjustment for head bumps will not include the attempt to counteract low frequency gain variations in the electronics.

Equalization feedback is routed from the output of the third stage to the emitter of the first stage. The third stage collector was chosen rather than the emitter (output) of the fourth stage because it is difficult, and at best unsafe, to encompass four stages with feedback. (There is danger of positive feedback and oscillations due to cumulative phaseshift. Any simple band limiting method of stopping oscillations arising from looping feedback around four stages generally results in distortion of the high audio frequencies).

Because of the loading effects (current requirements) of the feedback resistor upon the third stage, especially for the higher audio frequencies in 30-ips equalization, sufficient current must be provided in this stage to handle peak signals. (Clip level is 30 db above operating level in this preamp). This results in the dc base current requirement of Q3 being too high to be safely supplied directly from transistor Q1, and transistor Q2 is therefore provided in the circuit as a current amplifier. The current in Q2 is kept very low--only enough for the peak requirements of Q3--to ensure that Q2 does not add noise to the circuit.

The value of the current in transistor Q1 was optimized for lowest noise, one increment at a time, after all other parameters that affect the noise figure had been established (i.e. the heads to be used, and the resistances of the feedback elements<sup>(1)</sup>, which in turn were fixed by gain and load current requirements).

So much for equalization feedback, and gain and clip level. A number of other configurations would do the work. However, no circuit is useful if it causes surge current through the reproduce head sufficient to magnetize the head to the extent that increases (however slight) are noted in noise or in even order harmonic distortion. A simple, but effective, precaution is taken here. Charging current is most likely to flow through C2 to the head (from the base of the first stage) if the base-emitter junction were forward biased before voltage was applied to the collector. In this circuit, forward bias from the base is derived from the emitter of the third stage, and cannot be developed until after the collector voltage of the first stage has risen to an effective level. As a further precaution, the sequence happens gradually (because of the time constant of C1 and R9) thus further reducing the charging current. This current is limited to three microamperes maximum surge when the unit is turned on or off. Repeated tests showed no magnetization from this cause. Incidentally, the dc bias scheme helps to minimize the short disturbances that also arise at the output when an amplifier of this type is turned on or off. In addition, this results in high temperature stability despite the low value of operating current in the first stage.

#### Reproduce calibrate and reproduce level controls (Figure 2)

The calibrate control was incorporated so that the user would not have to scribe the front plate, or use other markers, to indicate when the reproduce potentiometer was set to operating level. He merely preadjusts the calibrate potentiometer and sets the reproduce level pointer to the CAL mark.

As so often happens, there is a price for this convenience. Approximately 6 db of additional gain is provided from the normal setting of the calibrate potentiometer. This represents a 6 db loss in level, and the voltage amplifier which follows had to be designed to contribute correspondingly less noise. Transistor Q5 is an emitter follower, dc connected to the base of transistor Q6, in order to present a low source impedance to (and thus reduce the noise contributed by) transistor Q6. The current in Q5 is very low, being only the base current of Q6, so that the noise introduced by this stage is sufficiently low. In general, since noise power adds as the rms, the addition of two equal powers will result in noise increase of only 3 db. If two noise powers are separated by 11 db, an increase of only 0.4 db will result.<sup>(2)</sup> Actually, the increase in total noise by the inclusion of transistors Q5 and Q6 was not discernible. The noise in transistor Q6 could not be reduced without the aid of transistor Q5 because the source resistance is high and also because a relatively high current is required as standby for the high clip level specified. The gain provided by transistor Q6 is 11 db. The record level control, with a gain margin of 8 db, is located after this amplifier in the reproduce chain.

#### Line amplifier (Figure 2)

The next transistor, Q7, is a gain stage, and transistor Q8 is an emitter follower which is directly coupled to a class A power amplifier capable of over 28 dbm output before clipping. A class A

amplifier was chosen because good complementary pairs of transistors for class B operation were not available at reasonable cost before the design was consummated.

The output meter may be strapped for normal level operation at either +4 dbm or +8 dbm. The VU meter may be switched to read rf bias current in the record head. When this is done, resistor R37 is switched in series with the meter movement (after the rectifier) in order to attenuate the signal to an "on-scale" reading. Unless a large rf signal is provided to the meter rectifier, it does not operate with constant efficiency over the desired temperature range, and a resistor such as R37 is required to attenuate the rectified signal. Special connector lugs are provided at the rear of the meter, for this resistor.

### THE RECORD AMPLIFIER CIRCUIT

#### Record calibration circuit (Figure 3)

As in the reproduce circuit just covered, signal-to-noise and clip level cannot be forgotten. The equalization network and the circuitry of the record head amplifier are two areas where much design planning are required.

In the unbalanced bridge position of the input selector switch, the signal from the input jack is carried directly to the 100 K ohm record level control, and thence to an emitter follower with high input impedance. From here the signal branches to transistor Q11, an isolation amplifier that leads to the input-output monitoring selector switch. Record level calibration is accomplished by means of potentiometer R45. Isolation transistor Q11 is provided so that disturbances which might result from action of the monitoring selector switch will not be recorded on the tape.

#### Record equalization circuit (Figure 3)

The main route of the signal is to the record equalizer. This equalizer, like the reproduce equalizer, must be capable of being varied over the entire range of pre-emphasis dictated by the combination of tape speed, equalization, and tape characteristics previously mentioned.

Essentially, the equalization scheme is to attenuate the signal by 26 db in resistors R42 and R52, which constitute the series and shunt arms of the attenuator. This amount of attenuation is necessary because some tapes require audio frequency boost that would reach an early clip level unless previously attenuated. Across the series arm of this attenuator is a variable capacitor, which pre-emphasizes the high frequency audio signals. The degree of pre-emphasis is adjusted by varying the value of the capacitance (located in the plug-in equalizer housing). NAB equalizations also require

bass boost which is provided by capacitor C21 and resistor R53. Of course, C21 is a short circuit for mid-frequencies and higher, and does not affect response in these regions.

A survey of the available commercial compression-type variable capacitors showed that R42 could not be less than 110 K if the necessary range of equalization time constants was to be obtained by a single capacitor. A smaller resistance would have reduced the shunt arm proportionately, and since the shunt arm is the source resistance for the next stage, a lower value would have made the problem of noise reduction in that stage easier to solve. Figure 4 shows two typical ranges of equalization and the capacitance limits required to achieve them. In the curves shown, pre-emphasis -- which starts at 1.35 kc -- is very heavy. That which starts at 29.4 kc is virtually zero pre-emphasis, and can be considered constant current recording.

For CCIR and 30 ips recordings, no bass boost is specified in the record process. In these instances, capacitor C21 and resistor R53 are shorted out by a large capacitor which is also located in the plug-in equalizer housings for use with these types of recordings.

As mentioned before, the signal has been attenuated 26 db from the original level at the record level potentiometer. The lowest signal expected at the record input is -20 dbm. Therefore, the non-emphasized frequencies could be as low as -46 dbm level at the input of Q12. Hence, Q12 must be made a low noise stage. To assure a light load on the equalization network, so as not to modify the curves, the input impedance of Q12 must be high. The shunt arm of the equalization network, resistors R52 and R53, are made part of the dc biasing network of transistor Q12. This eliminates the additional load of one dc biasing resistor which would otherwise be required for the circuit.

#### Record head amplifier (Figure 5)

Transistor Q13, the next stage, was required at the input of Q14 for the same reason that transistor Q5 was necessary (that is, to reduce the noise added to the signal by Q14). Q14 is of necessity a high current stage and, as such, would add to the incoming noise if its source impedance were not held to a low level by transistor Q13.

Transistors Q15 and Q16 together form the record head amplifier. Transistor Q15 is located in the collector circuit of transistor Q16 and supplies all of the dc collector current required by Q16. The ac impedance seen by the recording head looking towards the power supply is virtually 47 K, the value of resistor R57. Looking towards ground from the head, the controlling impedance is feedback resistor R58, whose effective value is not much less than its actual value of 68 K in this low gain configuration. The output impedance is the value of these two resistors in parallel. The measured value was approximately 25 K. Therefore, the amplifier supplies constant current to the record head to a much higher frequency than is necessary for recordings up to

18 kc, and the capability for recording to a much higher frequency is present if it should be required. The inductance of the record head is 5 mh.

This concludes the discussion on the signal amplifying portions of the electronics. The remaining circuitry is equally vital to a tape recorder, and required careful design for professional quality performance.

#### Erase and bias oscillator

The erase and bias oscillator has special requirements placed upon it. One of these is that the even order distortion in the rf power it produces must be less than 0.1 percent. A bias symmetry control permits balancing the oscillator so that it meets this requirement. A capacitor connected from the base to emitter of each oscillator transistor makes the balance surer. The effect of asymmetry in the bias oscillator output would be to produce an increase in noise and in second harmonic distortion. Distortion of 0.1 percent in the bias current is the most that can be tolerated. The symmetry is also kept within this limit when multitrack recordings are being made and two or more bias oscillators are locked together in frequency.

Because of the requirement for exceptional symmetry in rf bias current, a special test circuit has been built for conveniently measuring the distortion. The circuit is shown in Figure 6.

The symmetry bridge is operated as follows: a calibrating reference is first established by half wave rectification of the bias signal being sampled.

The imbalance between the positive and negative peaks of the bias signal is then measured by rectifying them in two closely matched diodes connected in a bridge circuit. This is done with the diodes first in one polarity and then with both diodes reversed. A balancing potentiometer is used to obtain equal positive and negative readings on a center reading voltmeter before and after the reversal. Either of these readings represents the degree of even order distortion when compared with the reference.

#### Record mode switching circuit (Figure 7)

Another requirement is that the oscillator output rise and fall at the proper rate when the recording is started and stopped.

In general, this timing is accomplished by means of dc switching transistor Q23, together with capacitors C44 and C43B and their associated resistors in the base circuit.

When the record amplifier is placed in the record mode, terminal 51 of the record relay is connected to the +23 volt line. Capacitors C43B and C44 charge through resistors R80 and R81, and transistor Q23 reaches full conduction in about 0.2 second -- slow enough so that turning on the oscillator does not cause a popping sound at the start of the recording. Transistor Q23 permits the use

of larger timing resistors, since they are located in the low current base circuit, so the size of the time constant capacitors need not be inordinately large. When the record process is stopped, the oscillator output should ideally decay at about the same rate that the tape stops. For this purpose, capacitor C43B with resistors R82, R80, and R79 in series provides a turn-off time constant of about .02 second .

The record amplifier also should start without producing extraneous sounds in the recording. Capacitor C43C, in series with resistors R83 and R80, and aided by capacitor C44 provides the desired time constant. When the record amplifier is turned off, diode CR11 blocks conduction in the reverse direction, and capacitor C43C prevents the abrupt turn off that would cause a recorded disturbance.

### POWER SUPPLY

The power supply, shown in Figure 8, is conventional in all respects except for short circuit protection feature. The series regulating power transistor is Q20; its current driver is transistor Q21 and the error voltage amplifier is transistor Q22. Zener diode CR10 is the reference diode. Current for the voltage amplifier and the series transistor are provided by a fourth transistor Q19. This transistor has its base-to-unregulated line voltage fixed by diodes CR7 and CR8. The emitter voltage is the voltage across resistor R73, and this voltage is lower than the base voltage so that Q19 is normally conducting. In case of an overload current, however, the increased voltage drop across the current sensing resistor R74 is transmitted through CR9 to the emitter, rendering the emitter voltage greater than the base voltage, and transistor Q19 is turned off. This shuts off the supply of current to the base of transistor Q20, thereby limiting the output current to a safe value. The current limit on the application of a short circuit is approximately 0.6 ampere.

### TEST RESULTS

In operation, the solid state design exceeds the essentials for professional tape recorders, and typical test results will now be discussed.

In Figures 9 A and B, total harmonic distortion of the tube and transistor amplifiers is plotted against line output. At mid-frequency, the performances are approximately equal, but there is less distortion and greater overload margin in the new circuit at the low and high frequencies. The clip level is a minimum of +28 dbm, and most units have a top level of +30 dbm.

Figures 10 A and B show total harmonic distortion plotted against record current. There is considerable reduction in distortion at all frequencies in the transistor version. The clip level is at least 26 db above the operating level.

In Figure 11, the vertical scale represents the noise power in a bandwidth of one cycle per second expressed in db below operating level (3). The top curve is a plot of total noise power response of the playback of tape which was recorded with no signal. Total noise can be divided into two components: (1) electronic noise power response (bottom curve), which is the noise of the reproduce amplifier with tape motion stopped; and (2) biased tape noise which is the rms difference of total noise and electronic noise. The position of the plot of biased tape noise (for the greater part well above electronics noise) indicates that the audible (total) noise of recorded tape is produced primarily by the tape for all frequencies except those above 15 kc. The electronic noise is equal to or higher than tape noise above this frequency only, where total noise and electronic noise are 3 db or closer to each other. The unweighted noise in a 20-cps to 22-kc bandwidth is 62 db or more below operating level.

These plots were made at 15-ips tape speed and with NAB equalization. Half track heads were used with 3M No. 201,  $\frac{1}{4}$ -inch-wide tape.

The regulated power supply permits operation with no deterioration with line variation of 105 to 125 vac. The electronics were tested between the temperature limits of 0°C to 75°C with only a slight reduction in the line amplifier clip level at the higher temperature.

There was no increase in noise at the higher temperature, certainly attesting to the low noise quality of silicon planar transistors which are used in all of the voltage amplifying stages.

### CONCLUSION

The development of silicon planar transistors has made possible the design of circuits that are simple to stabilize and that exhibit low noise over a wide temperature range. However, a degree of care is necessary to make very sure that there is adequate dynamic range in every stage of the amplifier, especially when a wide range of equalization or gain control is specified. Transistor stages that must be biased for higher current than is optimum for the electronics noise considered permissible at that point require special treatment. The steps taken to guarantee that noise is not added in these areas has been discussed. Also covered are the provision for exceptional balance in the bias oscillator, special switching for the oscillator, and the regulated power supply all of which are included for high performance in the Ampex Model AG-350. There are other features to be sure but only those which involve transistor methodology have been stressed.

The author wishes to credit the audio engineering management and staff for establishing the ambitious design goals and bringing into being a unit that meets these goals. Sincere thanks go to each member for his help in the preparation of this paper.

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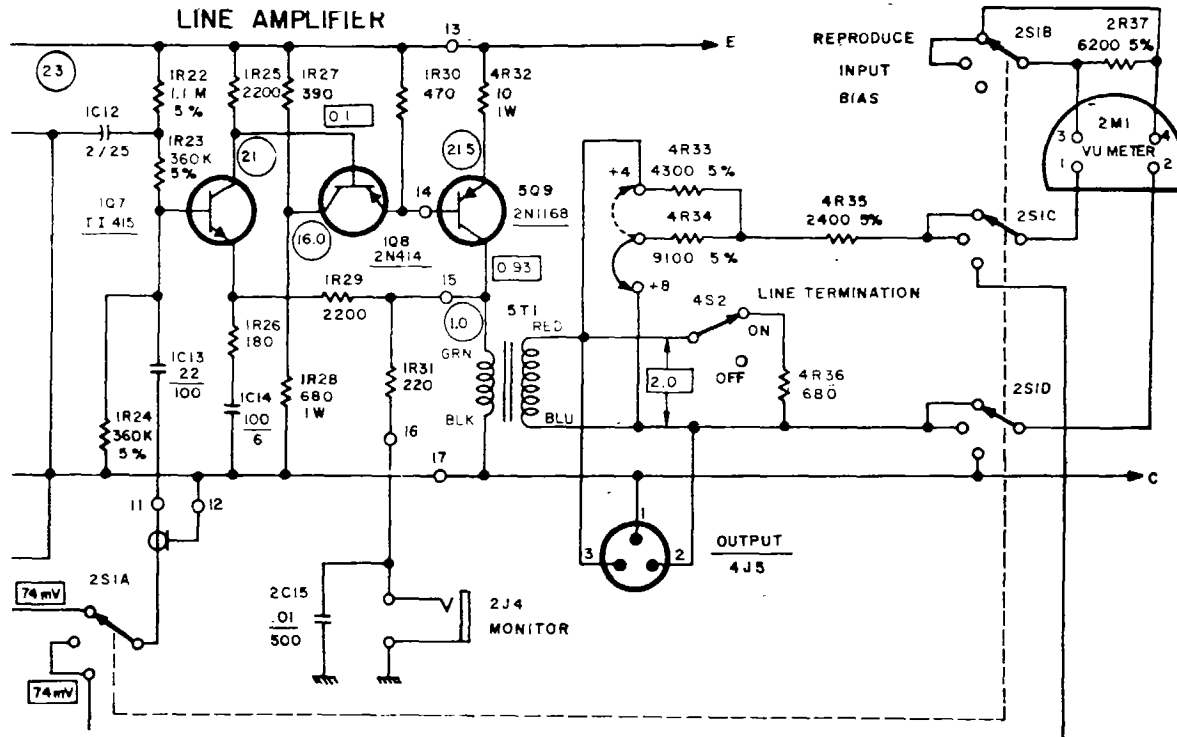


Fig. 2 LINE AMPLIFIER

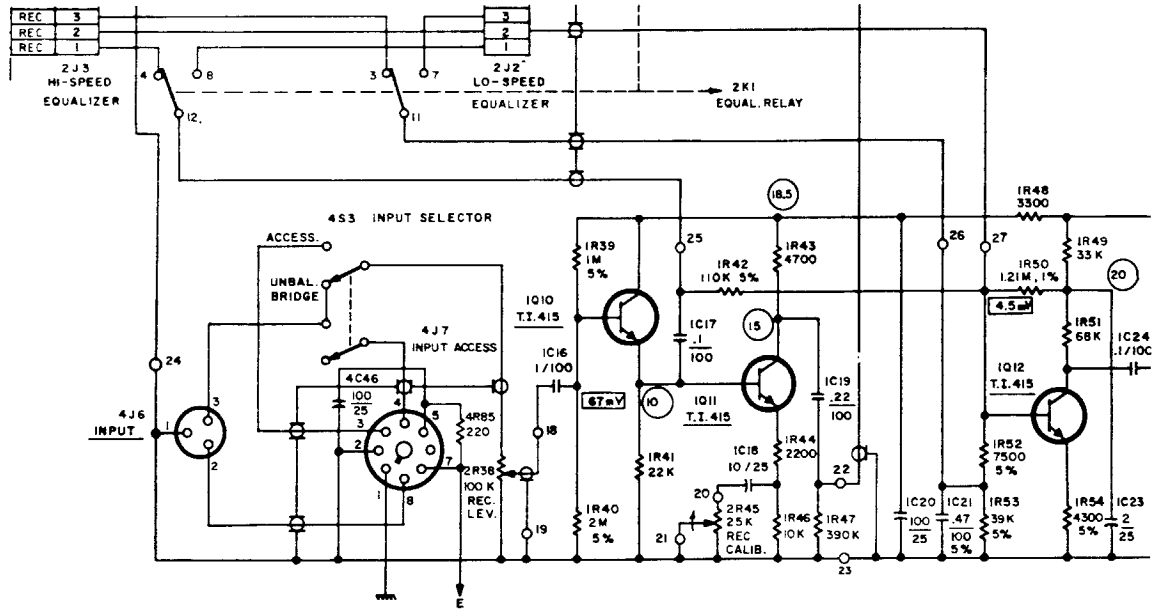


Fig. 3 RECORD INPUT AND EQUALIZATION

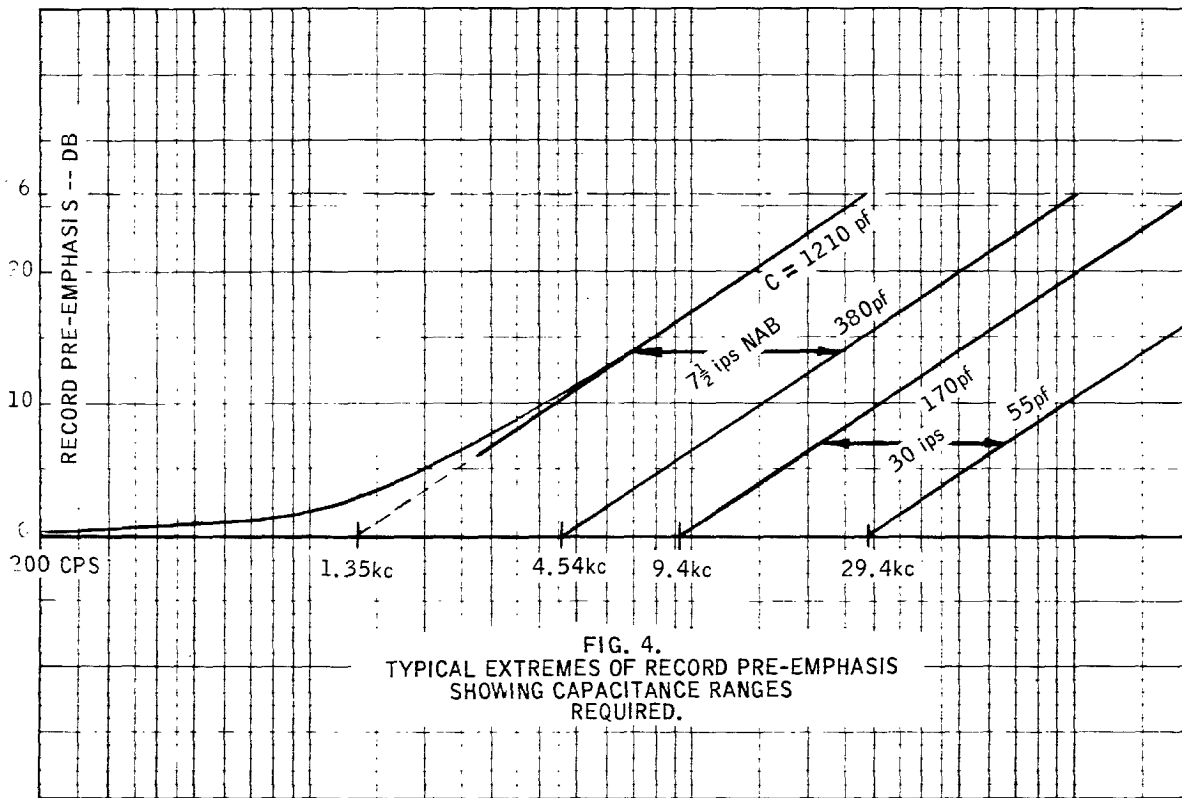


FIG. 4.  
TYPICAL EXTREMES OF RECORD PRE-EMPHASIS  
SHOWING CAPACITANCE RANGES  
REQUIRED.

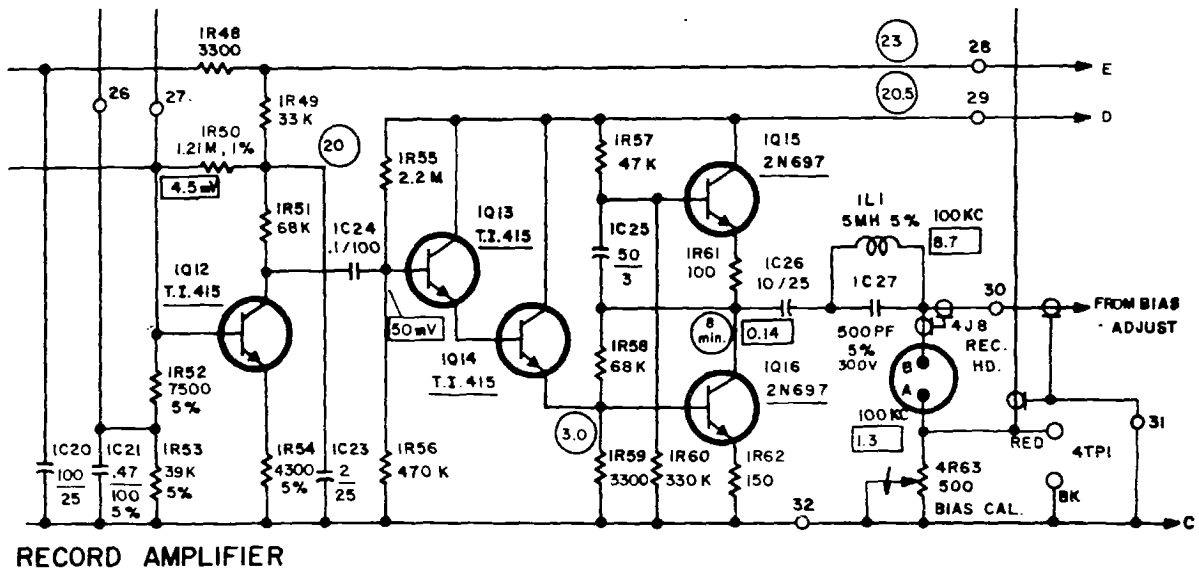


Fig. 5 RECORD AMPLIFIER

# BIAS SYMMETRY BRIDGE

## SCHEMATIC

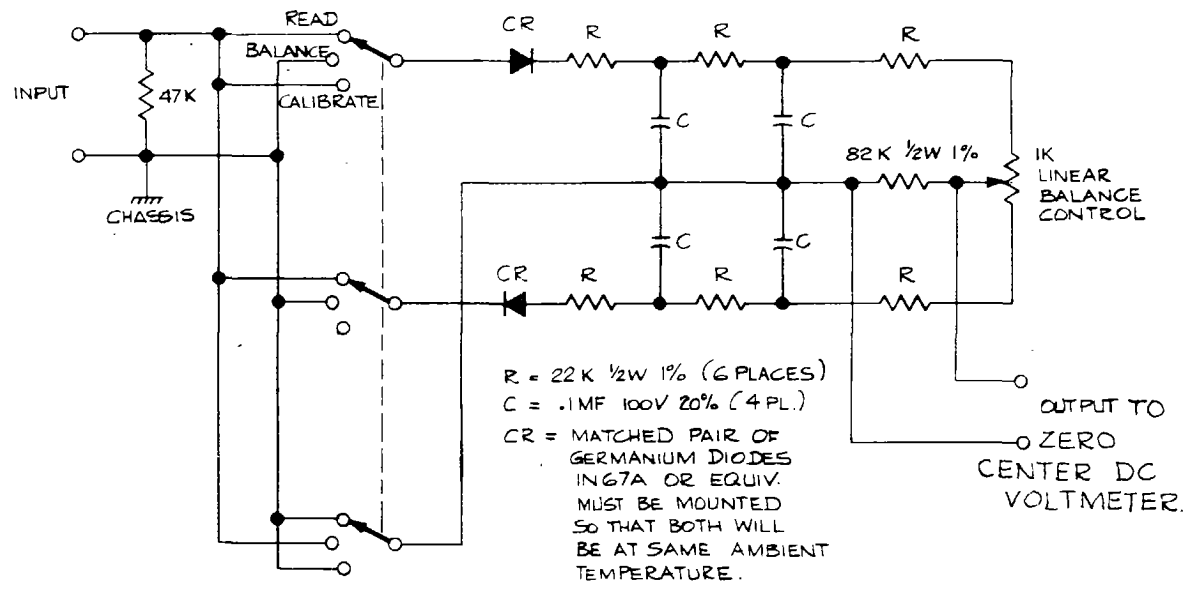


Fig. 6      BIAS SYMMETRY BRIDGE

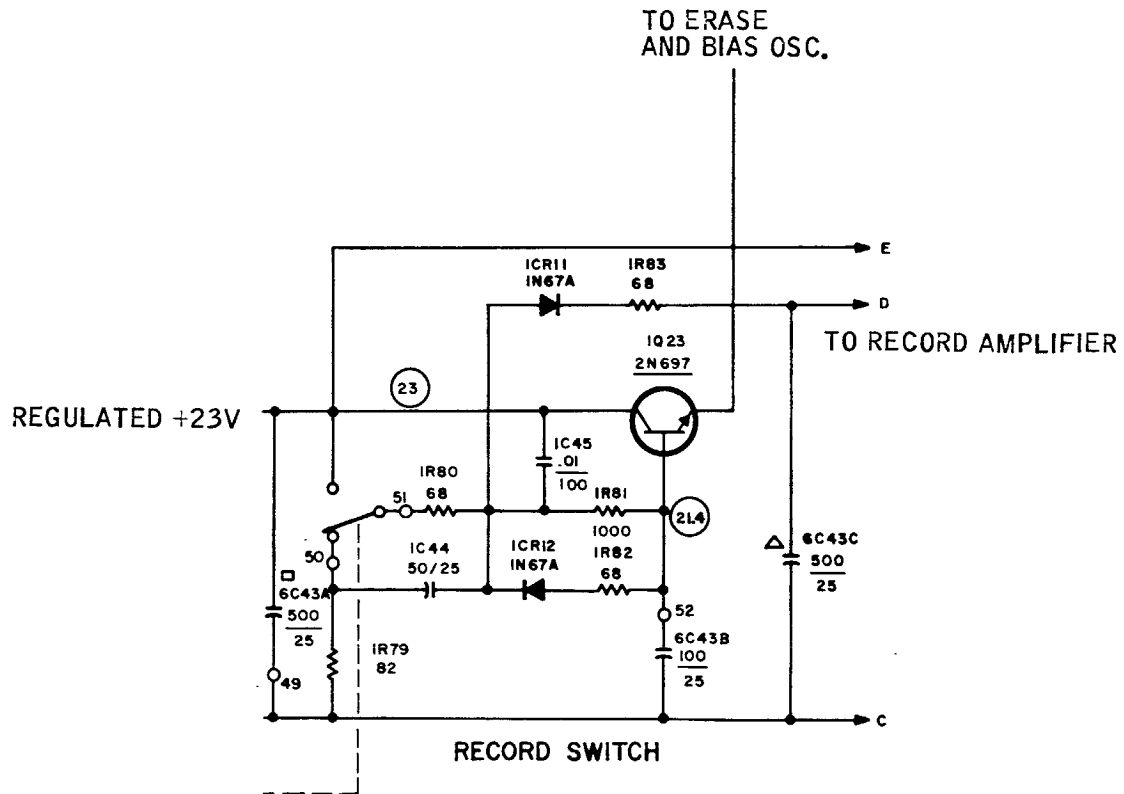


Fig. 7 RECORD MODE SWITCHING



FIG. 9A. LINE AMPLIFIER DISTORTION

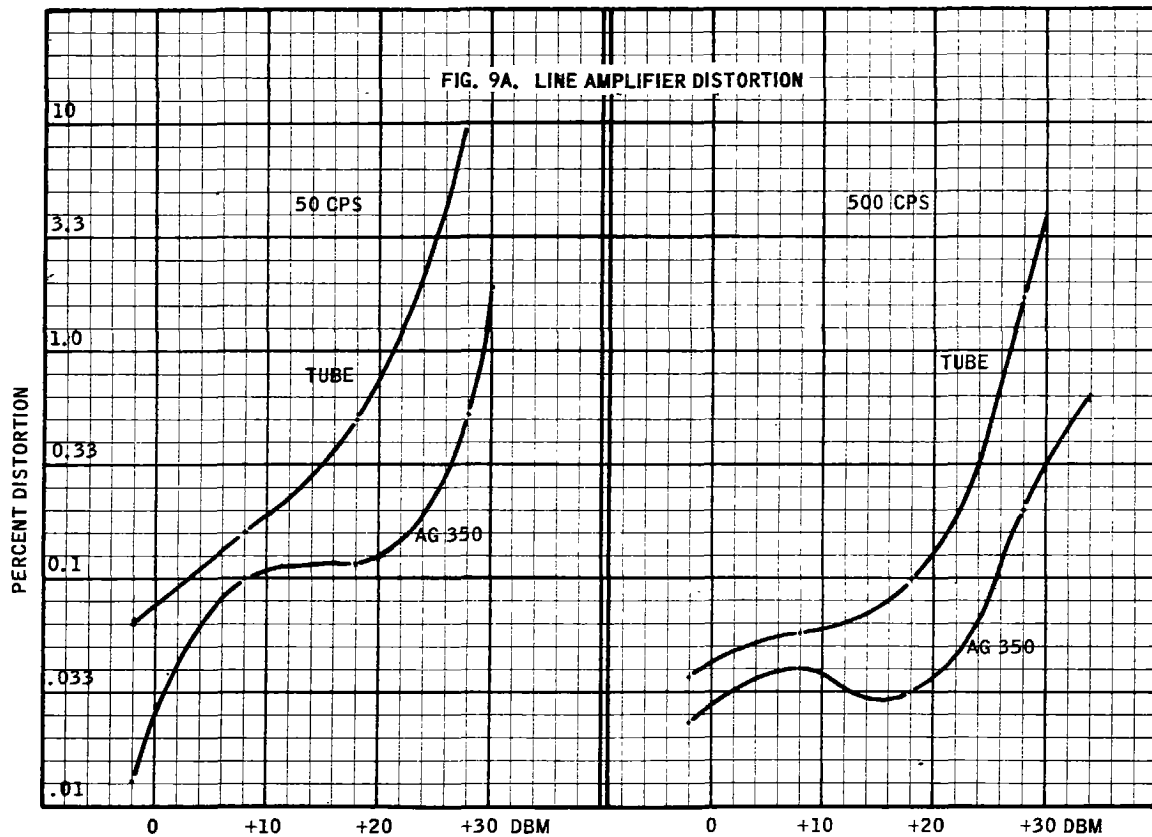


FIG. 9B. LINE AMPLIFIER DISTORTION

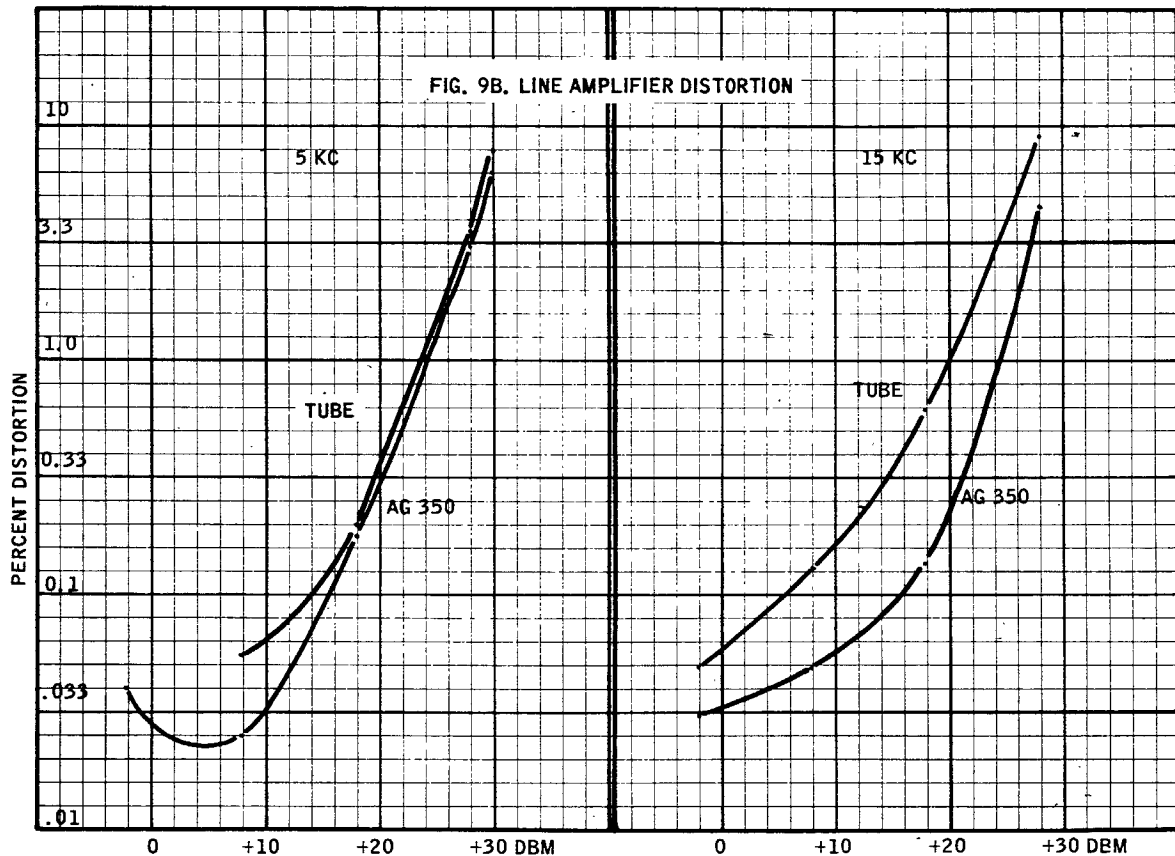


FIG. 10A. RECORD AMPLIFIER DISTORTION

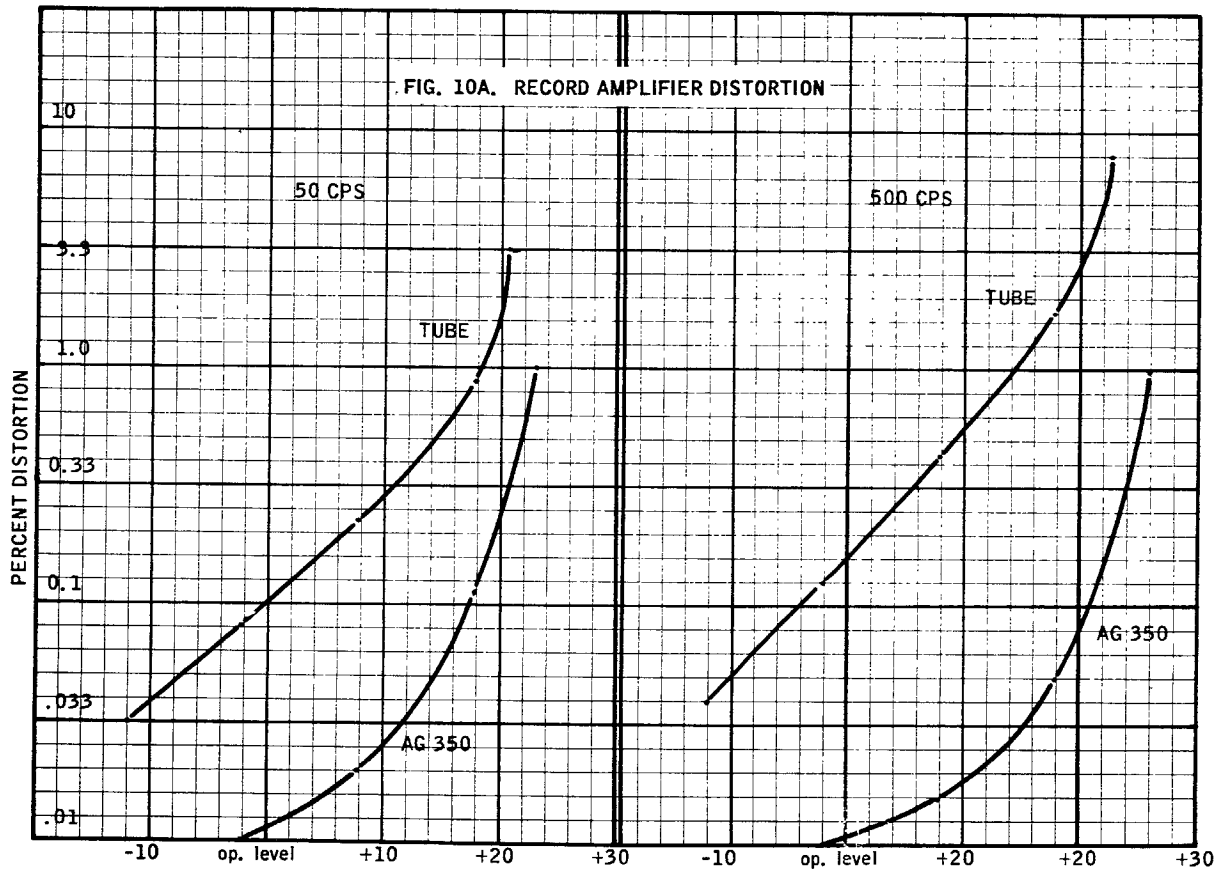
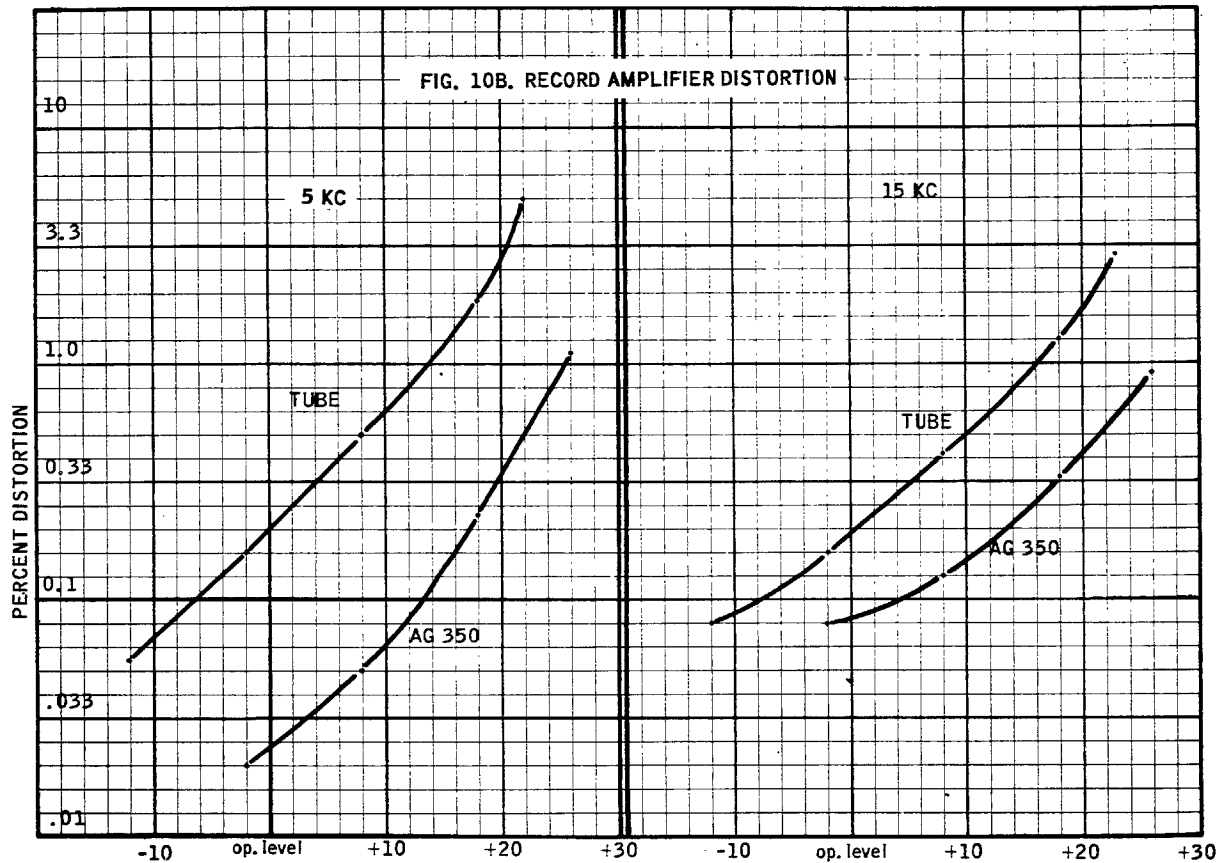


FIG. 10B. RECORD AMPLIFIER DISTORTION



AMPEX

NOTE: SMALLEST DIVISION IS 1 DB.

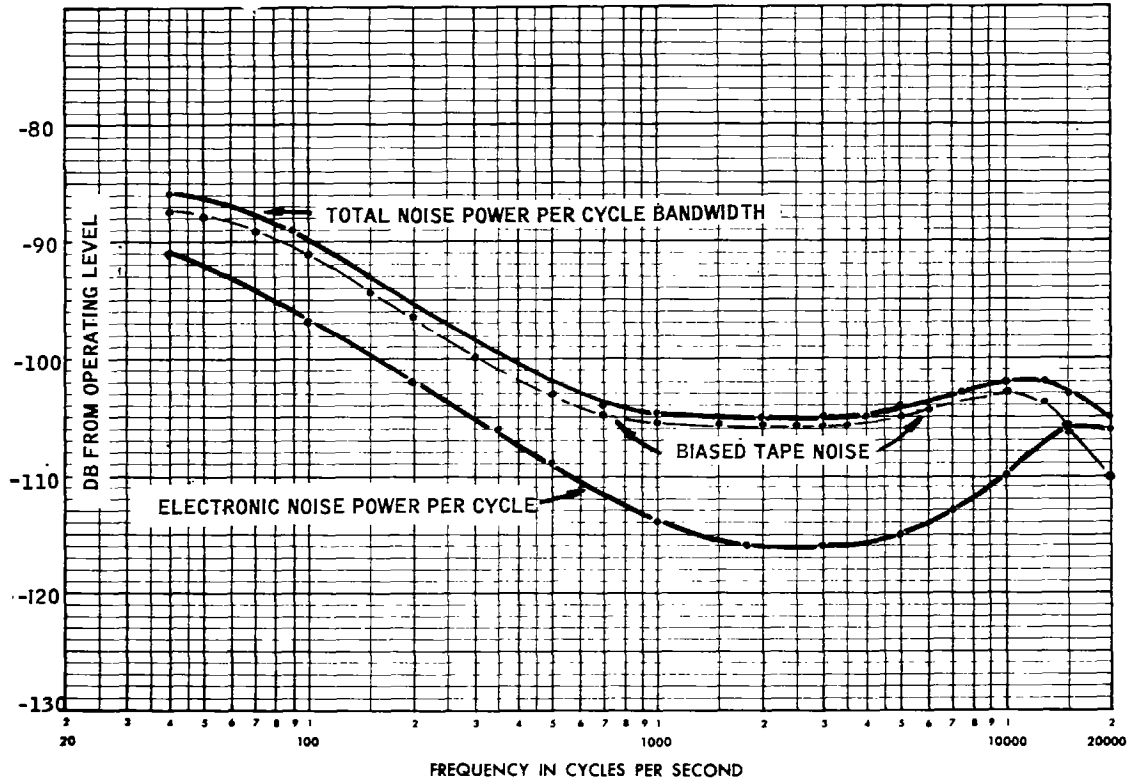


FIG. 11. BIASED TAPE NOISE AND ELECTRONIC NOISE